PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Docket No: Q78036
Isao OKADA, et al.	
Appln. No.: 10/693,928	Group Art Unit: 2627
Confirmation No.: 4142	Examiner: Latanya BIBBINS
Filed: October 28, 2003	

For: RECORDING PULSE GENERATOR

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellant submits the following:

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I. REAL PARTY IN INTEREST

Based on the information supplied by the Appellants, and to the best of Appellants' legal representatives' knowledge, the real party in interest is the assignee, ROHM CO., LTD.

II. RELATED APPEALS AND INTERFERENCES

Appellants, as well as Appellants' assigns and legal representatives, are unaware of any appeals or interferences which will be directly affected by, or which directly affect or have a bearing on, the Board's decision in the pending case.

III. STATUS OF CLAIMS

Claims 1-16 are all the claims pending in the present application. Claims 1-16 have been finally rejected, and are the subject of this appeal. The pending claims are set forth in the Appendix.

IV. STATUS OF AMENDMENTS

At the time of filing the original application on October 28, 2003, Appellants filed a Preliminary Amendment that amended the original claims and added new claims 6-16 and was entered. Appellants filed an Amendment Under 37 CFR 1.111 on November 20, 2006, which amended claims 1, 2, 4, 5 and 7-16, and was entered. A response under 37 CFR 1.116 was filed on April 30, 2007 but did not amend any claims. On the basis of the content of the Advisory Action dated May 22, 2007, it appears that the response was entered.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 1, the only independent claim pending in the application, defines the invention as a recording pulse generator comprising several elements and, with respect to the disclosed embodiment of Fig. 1, include "a first delay line," which corresponds to the delay line 11, having plural circuit elements cascaded in multiple stages. The delay line outputs several "output pulses," as explained at page 11 of the original application. Claim 1 further states that (1) the delay line outputs "output signals" and (2) that the output signals are "input to a level shift stage that shifts the levels of the plural output clocks to generate plural fine clocks, respectively." This latter feature corresponds to the parallel arrangement of inverting amplifiers, each having an output to a respective level shifter (LVS 22). As is clear from Figure 1, in response to the control signal Vs that is output by the PLL oscillator 1, the plurality of fine clock signals T0-T15 are generated.

In addition, claim 1 affirmatively requires a selector that "selects an arbitrary fine clock from plural fine clocks generated." This corresponds to the multiplexer 25a, as clearly explained at page 12, lines 7-10 and page 12, line 27 - page 13, line 10 of the original application. The use of a multiplexer as the "selector" is recited in dependent claims.

Finally, claim 1 requires a "recording pulse generator." The generator is operative to generate a recording pulse "on the basis of a fine clock selected." As explained at page 12, line 28 - page 14, line 3, the selected clock is input to flip-flop 25b, along with a data signal DA and an enabling signal ERA. As explained at page 13, line 11 with regard to Fig. 4, the data signal DA1 and enabling signal ERA1, an appropriate timing causes the flip-flop 1 to operate at the timing of the selected fine clock and generate a first recording pulse output (APC1).

Dependent claim 2 adds the "PLL oscillator" to claim 1, and is supported by Fig. 1 and the description at pages 11 and 12. The recited PLL oscillator has an oscillator (VCO2) that has plural circuit elements cascaded in multiple stages (2a), compares (4) a phase of a signal generated by the oscillator with the phase of the clock (EFMCLK) inputted to the first stage of the delay line, and controls a voltage (VS) of a power supply line for the first delay line (11) and the oscillator of the PLL oscillators according to the phase comparison result.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Claims 1 and 4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Publ. No. 2002/0051415 to Iijima ("Iijima") in view of what the Examiner characterizes as Appellants Admitted Prior Art ("AAPA");

(2) Claims 2, 3, and 6-9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Iijima in view of what the Examiner characterizes as AAPA, and U.S. Patent No. 6,493,305 to Hayashi et al. ("Hayashi");

(3) Claims 5 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Iijima in view of what the Examiner characterizes as AAPA and U.S. Patent No. 5,818,805 to Kobayashi et al. ("Kobayashi")

(4) Claims 10, 11, and 13-16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Iijima in view of what the Examiner characterizes as AAPA, Hayashi, and Kobayashi.

VII. ARGUMENT

Appellants respectfully submit that the claimed invention is patentable because (1) the background disclosure in the specification does not constitute an admission of statutory "prior art" and the Examiner has erroneously characterized the disclosure as Appellants' Admitted Prior Art (APAA), (2) in the absence of the erroneously characterized disclosure as prior art, the Examiner's rejection cannot stand by the Examiner's own admissions, and (3) even if the disclosure is prior art, the combination of references would not have rendered obvious the claimed invention in claims 1 and 2, and the claims dependent therefrom.

I. Appellants' Specification Does Not Disclose Statutory Prior Art"

The Examiner asserts that the Background of the Invention section of the Specification at pages 4-8 and FIG. 13 have been admitted as "prior art" or, in the alternative, that the admission of "conventional art" can be a basis for rejection.

No Admission of "Prior Art"

Neither the title, the text or the content of the specification and drawings admit that the disclosure at pages 4-8 and Fig. 13 are statutory "prior art." Just the contrary, the text clearly states that the disclosed structure is NOT prior art.

The relevant portions of the Specification include: the "Background of the Invention" section, which is labeled "Description of the Related Art." The term "prior art" is not used at all to describe the background art in Fig. 13. The text only refers to the disclosed structure as "conventional" (page 4, line 12). Moreover, the text expressly states that FIG. 13 "is not known as a prior art document" (page 4, lines 13 and 14). Finally, the text expressly states that "with regard to the present invention, any disclosed document of prior art was not found" (page 8, lines 5 and 6).

In short, Appellant has given no indication at any time from filing of the application to this submission that the disclosure in the Background section is prior art. Indeed, Appellant has intentionally avoided use of the term "prior art" and has consistently maintained that the "conventional art" is not prior art.

Related Art and Conventional Art is not an Admission of Prior Art

Subsection 2 under Background of the Invention is entitled "Description of the Related Art." The description of the background technology in that subsection includes a description of a "conventional recording pulse generator" that is illustrated in Fig. 13. As previously noted, that description of the conventional recording pulse generator expressly disclaims the structure as being prior art. The term "related" does not give any hint of an admission of that the disclosed technology was even prior to the claimed invention.; indeed, it could even have been developed subsequently but is useful to demonstrate an effective feature of the invention. Similarly, the term "conventional" is defined in the American Heritage College Dictionary as something "based on or in accordance with general use or practice; customary," and as used in an invention disclosure, is descriptive of the basis of an invention. The use of the word alone does not signify a concession of prior art status and, in the present case, any possibility of such suggestion is overcome by the express disclaimer of the illustrated figure as prior art , as noted above.

Case Law is Contrary to Examiner's Position

To Appellants' knowledge, there are no court or administrative decisions that support the Examiner's position. The only case law cited by the Examiner, *In re Nomiya*, 509 F.2d 566 (CCPA 1975), supports Appellants' position.

Specifically, the Examiner cites *In re Nomiya* for the proposition that the Background of the Invention section has relevant portions that constitute an admission of prior art. (Advisory Action Before the Filing of an Appeal Brief at page 3). The Examiner's reliance on *Nomiya* is completely misplaced.

In *Nomiya*, the patentees filed a patent application containing two drawing figures expressly labeled as "prior art" and accompanied by statements explaining the figures. The patentees were citizens and residents of Japan and had argued that the label referred to the status of the figures as prior art in Japan, not the United States, and pointed out that what may have been known in Japan "would not be prior art by virtue of any portion of 35 USC 102." *Nomiya*, at 570. However, the CCPA held that "[b]y filing an application containing Figs. 1 and 2, labeled prior art, *ipsissmis verbis* [in those very words], and statements explanatory thereof,

appellants have conceded what is to be considered as prior art in determining obviousness of their improvement." *Nomiya*, at 571 (emphasis added).

Only because the Appellants used the very words "prior art" did the Court accept the Examiner's position. In this special case, a showing of statutory basis under § 102 that the disclosure qualifies as prior art was not necessary.

In dramatic contrast, Appellants have not admitted that anything is "prior art", using those very words, and the narrow, but important, holding of *Nomiya* does not apply. Furthermore, the Examiner's argument that labeling the text "Description of the Related Art" verses "Description of the Prior Art" is an exercise in form over substance does not compel that *Nomiya* should apply. Appellants intentionally used the phrase "Related Art" or "Conventional Art" because the material disclosed in the background section is not known to be prior art. The use of the words "related" and "prior" is more than just form over substance because the words have drastically different meanings.[1] This difference has been used by Appellants and accepted by the USPTO for decades as being well understood.

Nomiya is very specific about requiring that the patentee state that the disclosure is "prior art", *ipsissmis verbis*, because only then has the patentee admitted that something was prior art. *Nomiya* is based upon an acknowledgment by the Court that Appellants can describe background art in a manner that helps understand the inventive advance, without facing a rejection on the basis of that background, unless there is an express statement admitting that the disclosure is prior art. To substitute the words "related" for "prior" as the Examiner proposes is contrary to *Nomiya's* premise. Neither *Nomiya* nor other Court decisions support the Examiner's application of Appellants' disclosure as prior art.

For example, in *Hellsund*, the patentee had admitted that certain disclosures in the Opel patent had been invented prior to his invention. *In re Hellsund*, 177 U.S.P.Q. 170 (CCPA 1973).

[1] "Related art" means art that is close to ones claimed invention while "prior art" has special meaning under § 103 which means art that can be used in determining obviousness of an invention. "Related art" is not necessarily "prior art", e.g., if the art was published after a critical date.

The majority relied on the patentee's response expressly saying that the prior invention was prior art. Clearly, there is no such admission in this case. More notably, however, in *Hellsund*, the concurring opinion by Judge Rich emphasized the need for the Examiner to specifically demonstrate a statutory basis for considering the Opel disclosure as prior art. Judge Rich stated that "[a]dmitted prior *invention* is not necessarily 'prior art' under § 103", and that important safeguards carefully written into § 102 would be discarded if the statutory basis was not analyzed, such as § 102(g)'s requirement that there be no abandonment, suppression, or concealment. *Hellsund*, at 174. Similarly, a statutory bar under either § 102 (b), (c), or (d) has been required in order for a patentee's own invention to constitute prior art for him regardless of whether the patentee admits knowledge of his own work. *Reading & Bates Constr. Co. v. Baker Energy Res. Corp.*, 223 U.S.P.Q. 1168, 1171-72 (Fed. Cir. 1984).

No Identified Statutory Support

The Examiner does not state under what statutory basis the Appellants' disclosure qualifies as prior art, and the Examiner only summarily states that referring to the structure as "conventional" constitutes prior art. Without such statutory support, the Examiner's position cannot be maintained. Furthermore, on the basis of Judge Rich's opinion in *Hellsund,* admitted "prior invention" is not necessarily "prior art," *and* admitting that something is "conventional" does not necessarily admit it is prior art.[2] Therefore, since the Examiner has not and cannot show any statutory basis under which the disclosure qualifies as prior art, the use of the word "related" or even "conventional" cannot be deemed as admission that the Background structure is prior art.

[2] Appellants note, similar to what the Appellants point out in *Nomiya*, that the inventors are from Japan, and that what is known or conventional in Japan would not be prior art by virtue of any portion of 35 U.S.C. § 102. Appellants do not state where or when the disclosure is conventional, but Appellants do state that, at least with respect to the U.S., FIG. 13 "is not known as a prior art document". (emphasis added) The accuracy of this statement has been confirmed by Appellants throughout the prosecution of the application.

II. Claim Rejections - 35 U.S.C. § 103

A. Claims 1 and 4 are not unpatentable under 35 U.S.C. § 103(a) over U.S. Publ. No. 2002/0051415 to Iijima ("Iijima") in view of what the Examiner erroneously characterizes as Appellants Admitted Prior Art ("AAPA");

Claim 1

Appellants respectfully submit that the claimed invention as set forth in claim 1 would not have been rendered obvious in view of the combinations of the cited prior art.

The Examiner asserts that Iijima discloses a recording waveform generator that includes a delay line with a plurality of delay elements connected in series which receives a first clock signal, a selector for selecting one delay clock signal from the delay clock signal group and a recording waveform generation circuit 18, as illustrated in Figs. 1 and 3. Appellants have assumed that the Examiner considers the delay line to be element 11a and the selector to be element 12 in Fig. 13. Appellants also note that in the embodiment of Fig. 13, a phase adjustment section 40 receives a clock signal at a PLL circuit 41 and provides it to a shift register 42 and selector 43 prior to input to the delay line 11 and selector 12.

The Examiner points to the disclosure in paragraphs [0014] and [0033] as containing pertinent teachings. In particular, the Examiner points to the delay line as being an equivalent to a structure that "generates plural fine clocks." However, claim 1 defines the delay line as producing "output signals" and a "level shift stage" as producing the fine clocks. Indeed, the Appellants' own specification teaches this difference at page 11 where it states:

> Although the conventional recording pulse generator implements the OR operation of the selected clock from the delay line 11 and the EFMDATA-1T to attain the recording pulse, the recording pulse generator of this embodiment delays the EFMCLK by the delay line 11, namely, generates a delayed signal (fine clock) of the EFMCLK by utilizing the ring oscillator VCO composed of the inverter 2b, as described above, and controls a recording pulse generator 25 by the signal (fine clock) to generate a recording pulse.

Thus, the Examiner's analysis is not correct and the Examiner's analysis cannot support the rejection.

In addition to the absence of the level shift stage, Appellants submit that there is no teaching that the clocks in Iijima are "having different phase differences with a clock inputted to the first phase of the first delay line, according to the number of stages of the plural circuit elements thereof."

In short, the absence from Iijima of "a level shift stage that shifts the levels of the plural output clocks to generate plural fine clocks, respectively," as set forth in claim 1 clearly distinguishes Iijima from the claimed invention. Further, such feature would not be inherent, as it would not necessarily flow from the delay line in Iijima.

The Examiner clearly acknowledges these deficiencies in Iijima, as he finds it necessary to expressly add the Background of the Invention teachings to support an obviousness rejection. Further, the Examiner expressly admits that Iijima fails to teach a level shift stage that generates the plural fine clocks to be selected by the selector. Thus, if the AAPA is excluded as qualified prior art that can support the rejection, the invention is patentable over Iijima.

Even if the AAPA is included in the rejection, Appellants respectfully submit that the illustrated level shift stage 22 in Fig. 13 of the present application does not teach or suggest that the level shift stage may be used to generate fine clocks to be selected by the selector. As explained by the Appellants in the specification at page 11 when distinguishing the structure of Fig. 13 from the embodiment of the invention in Fig. 1, "the recording pulse generator of this embodiment delays the EFMCLK by the delay line 11, namely, generates a delayed signal (fine clock) of the EFMCLK by utilizing the ring oscillator VCO composed of the inverter 2b, and controls a recording pulse generator 25 by the signal (fine clock) to generate a recording pulse.

Based at least on the absence of the claimed source of fine clocks in the combination of AAPA and Iijima, reversal of the rejection is respectfully requested.

Claim 4

This dependent claim specifies that the selector of claim 1 is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks. The Examiner argues that Iijima discloses a selector selecting one delay clock signal from the delay clock signal group, on the

basis of the disclosure in paragraph [0014]. The Examiner states that a selector is a switch that connects to multiple lines "as equivalent to a multiplexer."

Appellants respectfully submit that the claim is patentable for the reasons given for parent claim 1. Moreover, a "multiplexer" is expressly required. The Examiner admits that no multiplexer is taught in Iijima. Instead, the Examiner states that the structure in Iijima is "equivalent." There is no description by the Examiner of how there is an equivalence to a multiplexer, or how or why the structure can be converted to be a multiplexer, as required by the recently issued USPTO Guidelines for Obviousness, consistent with the *KSR* decision. Further, Appellants respectfully submit that there is no teaching of the function that the selection signals are shifted in the same phase with the fine clocks. Paragraph [0014] in Iijima makes no mention of such coordinated shifting.

Thus, reversal of the rejection is respectfully requested.

B. Claims 2, 3, and 6-9 are not unpatentable under 35 U.S.C. § 103(a) over Iijima in view of what the Examiner erroneously characterizes as AAPA and U.S. Patent No. 6,493,305 to Hayashi et al. ("Hayashi");

Claim 2

The invention defined by claim 2, which depends from claim 1, would not have been rendered obvious in view of the combinations of the cited prior art. Again, with the exclusion of the AAPA from this rejection, the rejection is deficient as neither Iijima nor Hayashi provide the teachings the Examiner needs from the AAPA in Fig. 13.

Moreover, even if the AAPA is utilized, none of the references teach that "the PLL oscillator compares the phase of a signal generated by the oscillator with the phase of the clock inputted to the first stage of the first delay line," as recited in Claim 2 of the present application.

Iijima

The Examiner notes that claim 2 is directed to the additional structure of a PLL oscillator and an EFM clock that is inputted to a first stage of the first delay line. The Examiner asserts that Iijima discloses the PLL oscillator and a clock inputted to the first stage but admits it does

not teach the specifics of the PLL oscillator or the EFM clock that varies according to a recording speed.

Hayashi et al

The Examiner looks to Hayashi et al for a teaching of a pulse width control circuit with a PLL oscillator having a voltage control oscillator, phase comparator and low pass filter that supplies a control voltage, with a plurality of delay cells as disclosed at col. 9, line 58, 59 and Fig. 9. The Examiner further notes that the phase comparator compares the phase of oscillator output in the reference signal at col. 9, lines 48-52 and that the low pass filter of the PLL oscillator supplies a control voltage Vt according to the phase difference signal, as disclosed at col. 9, lines 52-54. The Examiner also notes that the control voltage Vt from the low pass filter is supplied to the control terminal of both delay cells and both cells have the same circuit elements and configuration, as disclosed at col. 9, lines 66-col. 10, line 5. The use of EFM clocks is noted as well. Finally, the Examiner attempts to justify the combination of Iijima and Hayashi by asserting it would have been obvious to use a PLL oscillator and delay circuit with common circuit elements in a common supply voltage as described by Hayashi in the circuit of Iijima. The motivation is to overcome sensitivity to external effects such as power fluctuations. The Examiner also asserts it would have been obvious to use EFM clock inputs because errors are reduced. Further, since disks can be played or written at different speeds, the Examiner states that EFM data needs to be written to the disk at different speeds.

No Teaching of Level Shifting Stage

Appellants respectfully submit that these assertions by the Examiner involve a clear exercise in hindsight. First, Hayashi does not remedy the significant deficiencies of Iijima as already noted.

No Combination with Specified PLL Oscillator

Claim 2 adds the "PLL oscillator" to claim 1. The recited PLL oscillator (1) compares the phase of a signal generated by the oscillator with the phase of the clock inputted to the first stage of the delay line and (2) controls "a voltage of a power supply line for the first delay line and the

oscillator of the PLL oscillators according to the phase comparison result.". This is not taught in either prior art reference.

The Examiner admits that Iijima does not teach this feature, based on his reliance on Hayashi. Indeed, an output of the PLL oscillator of Iijima implements phase control of a signal outputted from "a delay line" (Paragraphs 55, 56 and Fig. 3).

The Examiner relies on the teachings of Hayashi at column 9, lines 46-52, to support the rejection. However, this text describes Fig. 9. In Fig. 9, "the phase of a signal generated by the oscillator" is compared with RFCK. Therefore, in the present application, "the phase of a signal generated by the oscillator" is compared with "the phase of the clock inputted to the first stage of the first delay line". The phase of the clock inputted to the first stage of the first delay line is that of EFMCLK as shown in Fig. 1 of the present application. In other words, EFMCLK is inputted both to the first stage of the first delay line and to PLL oscillator.

However, RFCK described in Hayashi is different from "the phase. pf the clock in inputted to the first stage of the first delay line" described in the present application, because SIN corresponds to "the phase of the clock inputted to the first stage of the first delay line" and SIN is not inputted both to the first stage of the first delay line and to PLL oscillator.

Further, the output Vt of the PLL oscillator disclosed in Hayashi does not control "a voltage of a power supply line", but it is inputted to the NMOS 107 connected in series with the inverter 101 constituting a delay cell (column 10, lines 30-40 and Fig. 10).

Accordingly, Iijima and Hayashi lack the disclosure of "PLL oscillator controls a voltage of a power supply line.... according to the phase comparison result", as stated in claim 2. As a result, even if Iijima and Hayashi are considered together, they cannot result in the configuration of the present invention as defined by claim 2.

No Motivation to Combine

As explained at page 8 of the present application with regard to the Summary of the Invention, the disclosed recording pulse generator is intended to freely vary the run length of the EFM data by means of a signal generator composed of the multiplexer and flip-flops. This way, plural signal processing may be accomplished with one delay line, by using the delay line in

common and only increasing the number of the recording pulse generators, as needed. The concern in Hayashi is simply with pulse width control in the environment indicated in Fig. 3 and Fig. 8. The goal is to compensate for delay circuits that are sensitive to external effects such as power fluctuations and temperature changes, as noted by the Examiner at col. 1, lines 50-56, and to attain short pulse widths. There is no concern with generation of multiple fine clocks with different phase differences.

Because of the difference in goals between Hayashi and Iijima, contrary to the Examiner's assertion, there would be no motivation for the combination of these references in the manner suggested, particularly in a manner that attempts to duplicate the invention of the present application.

Furthermore, even if combined, neither Iijima nor Hayashi discloses or suggests a recording pulse generator wherein a PLL oscillator compares (1) the phase of a signal generated by the oscillator with (2) the phase of the clock inputted to the first stage of the first delay line, as claimed in claim 2.

In Hayashi, the PLL circuit 3 compares the phase of the oscillation output signal with the phase of reference signal RFCK, which is not inputted into the first stage of the first delay line. *Hayashi* at FIG. 9 and col. 9 lines 39-57. Only the input signal SIN is inputted into the first stage of the first delay line. The input signal SIN is not compared by the PLL oscillator 3. In contrast, according to the invention, the EFMCLK is inputted into both the first stage of the first delay line and the PLL oscillator. (FIG. 1) Because the input signal SIN is not compared by the PLL circuit 3, and the reference signal RFCK is not inputted to the first stage of the first delay line, the combination of Iijima and Hayashi does not disclose or suggest all the recitations of claim 2.

Therefore, claim 2 is not rendered unpatentable by the cited references and respectfully request reversal of the rejection.

Claims 3 and 6-9

These claims would be patentable for the reasons given for their parent claims.

C. Claims 5 and 12 are not unpatentable under 35 U.S.C. § 103(a) over Iijima in view of AAPA and U.S. Patent No. 5,818,805 to Kobayashi et al. ("Kobayashi")

These claims provide a similar limitation to parent claims 1 and 4 and would be patentable for the reasons given for their parent claims. Kobayashi is merely cited for a teaching of a recording signal generating apparatus that uses a T-type flip-flop that is triggered by the output of a data selector, as illustrated in Fig. 16 and described at col. 12, lines 50 and 51. The Examiner asserts that the data elector 18 provides one of eight delayed clock outputs to the T-type flip-flop, as disclosed at col. 12, lines 28-36. The Examiner does not assert that Kobayashi has relevance to the above identified, and previously argued, deficiencies of Iijima.

Thus, the claims would be patentable for the reasons given for their parent claims.

D. Claims 10, 11, and 13-16 are not unpatentable under 35 U.S.C. § 103(a) over Iijima in view of AAPA, Hayashi, and Kobayashi.

The claimed invention as set forth in claim 10, 11 and 13-16 would not have been rendered obvious in view of the combinations of the cited prior art. These claims depend from independent claim 1 or dependent claim 2. Again, with the exclusion of the AAPA from this rejection, Appellants respectfully submit that the claims would not be unpatentable for the reasons previously given that distinguished claims 1 and 2 over Iijima alone or with the AAPA, and the reasons given for Hayashi and Kobayashi to be inadequate to remedy those deficiencies.

The Examiner characterizes claims 10-16 as being drawn to a recording pulse generator where the recording pulse generation means is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer. The Examiner notes that Iijima and Hayashi disclose a recording waveform generation circuit that processes data based on a delayed signal that is supplied from a selector but do not specifically teach the elements of the circuit. The Examiner points to Kobayashi for a teaching of a recording signal generating apparatus that uses a T-type flip-flop that is triggered by the output of a data selector, with reference to Fig. 16, element 18 and the disclosure at col. 12, lines 50 and 51. The Examiner notes that the data selector provides 1 of 8 delayed clock outputs to the T-type flip-flop, with reference to Fig. 16, element 10 and the disclosure at col. 12, lines 28-36.

The Examiner asserts that it would be obvious to combine the three references and, in particular to use a flip-flop to implement the function of the recording waveform generation circuit described by Iijima.

Appellants respectfully submit that Kobayashi does not remedy the deficiencies of Iijima alone or in combination with Hayashi, as already explained. Moreover, Kobayashi does not teach how and why a combination of the distinct structures of Hayashi should be inserted into the structure of Iijima. Kobayashi is merely cited for the teaching of the use of a flip-flop.

Appellant submits that it is the combination of components in these claims that results in the advantages disclosed in the application and forms the basis for the invention. It is this combination that is not taught or suggested in the prior art, other than to the Examiner's use of hindsight based on Appellant's own teachings.

Appellant respectfully requests reversal of the rejections.

Unless a check is submitted herewith for the fee required under 37 C.F.R. §41.37(a) and 1.17(c), please charge said fee to Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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CLAIMS APPENDIX

CLAIMS 1-16 ON APPEAL:

1. A recording pulse generator comprising:

a first delay line having plural circuit elements cascaded in multiple stages, wherein the first delay line outputs plural output clocks each having different phase differences with a clock inputted to the first stage of the first delay line, according to the number of stages of the plural circuit elements thereof;

a level shift stage that shifts the levels of the plural output clocks to generate plural fine clocks, respectively;

a selector that selects an arbitrary fine clock from the plural fine clocks generated; and

a recording pulse generator that generates a recording pulse on the basis of a fine clock selected.

2. A recording pulse generator as claimed in Claim 1, further comprising a PLL oscillator that possesses an oscillator with plural circuit elements cascaded in multiple stages, compares the phase of a signal generated by the oscillator with the phase of the clock inputted to the first stage of the first delay line, and controls a voltage of a power supply line for the first delay line and the oscillator of the PLL oscillators according to the phase comparison result.

3. A recording pulse generator as claimed in Claim 1, wherein the clock inputted to the first stage of the first delay line is an EFM clock that varies according to a recording speed.

4. A recording pulse generator as claimed in Claim 1, wherein the selector is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks.

5. A recording pulse generator as claimed in Claim 1, wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer.

6. A recording pulse generator as claimed in Claim 2, wherein the clock inputted to the first stage of the first delay line is an EFM clock that varies according to a recording speed.

7. A recording pulse generator as claimed in Claim 2 , wherein the selector is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks.

8. A recording pulse generator as claimed in Claim 3, wherein the selector is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks.

9. A recording pulse generator as claimed in Claim 6, wherein the selector is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks.

10. A recording pulse generator as claimed in Claim 2, wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer.

11. A recording pulse generator as claimed in Claim 3, wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer.

12. A recording pulse generator as claimed in Claim 4, wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

13. A recording pulse generator as claimed in Claim 6, wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer.

14. A recording pulse generator as claimed in Claim 7, wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

15. A recording pulse generator as claimed in Claim 8, wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

16. A recording pulse generator as claimed in Claim 9, wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

EVIDENCE APPENDIX:

Appellants are required to submit, pursuant to 37 C.F.R. § 41.37(c)(1)(ix), copies of any evidence submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132 or any other evidence entered by the Examiner and relied upon by Appellant in the appeal.

Appellants respectfully submit that there are no documents or other evidence submitted to the Examiner.

RELATED PROCEEDINGS APPENDIX

Appellants are required to submit copies of decisions rendered by a court or the Board in any proceeding identified about in Section II pursuant to 37 C.F.R. § 41.37(c)(1)(ii).

Appellants respectfully submit that there are no decisions identified in Section II

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Docket No: Q78036
Isao OKADA, et al.	
Appln. No.: 10/693,928	Group Art Unit: 2627
Confirmation No.: 4142	Examiner: Latanya BIBBINS
Filed: October 28, 2003	

For: RECORDING PULSE GENERATOR

SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. The statutory fee of $510.00 is being charged to Deposit Account No. 19-4880 via EFS Payment Screen. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

Respectfully submitted,

/Alan J. Kasper/

Alan J. Kasper
Registration No. 25,426

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